111, 113, 115 - 123 and 125 - 128 of the above application are deemed to read on elected "species" I.

With respect to Claims 65 - 67, 73, 74, 76, 110, 111, 113, 118 - 122, and 125, Figs. 8a - 8d (collectively "Fig. 8") and Figs. 10a - 10d (collectively "Fig. 10") of "species" I generally illustrate a varactor configured in accordance with the invention. One of the plates of the varactor is partially formed by an inversion layer which appears and disappears in stages during varactor operation. The staged inversion layer is produced by suitably adjusting various physical characteristics of the varactor. Figs. 8 and 10 are illustrated in such a way as to generally represent how all of these characteristics are adjusted to produce the staged inversion layer.

For instance, the staged inversion layer can be produced during varactor operation by suitably varying the gate dielectric thickness. Although Figs. 8 and 10 illustrate the gate dielectric thickness as being constant, paragraph 80 of the specification provides that the gate dielectric thickness can be varied in the varactor of Fig. 8 as described later (in the specification) in connection with certain implementations of the varactor of Fig. 8.

Variation of the gate dielectric thickness to produce the staged inversion layer in the varactor of Fig. 8 is further supported by the statement in paragraph 165 of the specification in connection with the varactors of Figs. 8 and 10 that "Examination of Eq. 33 indicates that threshold voltage V_{T0} for a gate portion can be adjusted by adjusting its gate dielectric thickness t_{GD} . . ." and by the statement in paragraph 168 of the specification that "Figs. 12 - 21 illustrate implementations, or variations, of the n-channel varactor of Fig. 8 in which portions of gate region 131 are provided with different zero-point gate-to-body threshold voltages V_{T0} in accordance with the invention by (a) variously dividing gate dielectric layer 110 into multiple portions of different thicknesses . . .". Dependent Claims 65 and 118, which are generally directed to having the gate dielectric layer comprise multiple portions of different respective thicknesses, thereby read on "species" I.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

The staged inversion layer can be produced during varactor operation by suitably varying the net dopant concentration of the surface depletion region. This is supported by the statement in paragraph 165 in connection with the varactors of Figs. 8 and 10 that "Examination of Eq. 33 indicates that threshold voltage V_{T0} for a gate portion can be adjusted by adjusting . . . net dopant concentration N_B in the surface depletion portion of that gate

portion . . ." and by the statement in specification paragraph 168 that "Figs. 12 - 21 illustrate implementations, or variations, of the n-channel varactor of Fig. 8 in which portions of gate region 131 are provided with different zero-point gate-to-body threshold voltages V_{T0} in accordance with the invention by . . . (b) providing portions of surface depletion region 126 with different values of average net dopant concentration N_B . . . ". Hence, dependent Claims 66 and 119, which are generally directed to having the surface depletion region comprise multiple portions of different average net dopant concentrations, read on "species" I.

Gate electrodes 112 and 162 of the varactors of Figs. 8 and 10 are illustrated very generally in Figs. 8 and 10. In contrast to the implementations of Figs. 12 - 17, 19, and 21 in which doped semiconductor layer 112L of gate electrode 112 is unshaded while metal layer 112U of electrode 112 has slanted shading, gate electrodes 112 and 162 have dotted shading in Figs. 8 and 10 to indicate that electrodes 112 and 162 in Figs. 8 and 10 can variously consist of doped semiconductor material and metal. This electrode construction is specifically supported by the statement in specification paragraph 81 that "Electrode 112 may consist of conductively doped semiconductor material and/or metal".

When the gate electrode contains doped semiconductor material, the staged inversion layer can be produced during varactor operation by suitably varying the conductivity type or/and net average dopant concentration of the doped semiconductor material. This is supported by the statement in specification paragraph 165 in connection with the varactors of Figs. 8 and 10 that "Examination of Eq. 33 indicates that threshold voltage V_{T0} for a gate portion can be adjusted by adjusting . . . the conductivity types of the polycrystalline semiconductor material in the portion of gate electrode 112 or 162 in that gate portion" and by adjusting "net dopant concentration N_{POLY} of the polycrystalline semiconductor material in the portion of electrode 112 or 162 in that gate portion".

Variation of the conductivity type or/and net average dopant concentration of the doped semiconductor material of the gate electrode to produce the staged inversion layer in the varactor of Fig. 8 is further supported by the statement in specification paragraph 168 that "Figs. 12 - 21 illustrate implementations, or variations, of the n-channel varactor of Fig. 8 in which portions of gate region 131 are provided with different zero-point gate-to-body threshold voltages V_{T0} in accordance with the invention by . . . (c) constituting gate electrode 12 as upper metallic layer 112U and lower layer 112L consisting of doped polycrystalline semiconductor material divided laterally into portions of both (n-type and p-type)

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

conductivity types " and by the immediately following statement in paragraph 168 that "Alternatively or additionally, polycrystalline semiconductor material of one conductivity type in lower gate electrode layer 112L can be laterally divided into multiple portions having different values of average net dopant concentration N_{POLY}". Consequently, independent Claim 107 and dependent Claims 67, 73, 74, 110, 111, and 120 - 122, which all are generally directed to having doped semiconductor material of the gate electrode comprise multiple portions of different conductivity type or/and different net average dopant concentration, read on "species" I.

As noted above, electrodes 112 and 162 of the varactors of Figs. 8 and 10 can variously consist of doped semiconductor material and metal and are illustrated very generally using dotted shading in Figs. 8 and 10 to allow combinations of doped semiconductor material and metal. Specification paragraph 81 states that "In some implementations of the varactor of Fig. 8, electrode 112 includes (as discussed below) laterally adjoining semiconductor portions of opposite conductivity type". In light of the way that gate electrode 112 is illustrated in Fig. 8 and what is said in the foregoing statement in paragraph 81, Claims 76, 113, and 125 directed to the gate electrode having a metal-containing layer for electrically shorting doped semiconductor gate electrode portions together reasonably read on "species" I.

For the reasons presented below, Applicants' Attorney believes that the remainder of the pending claims, i.e., Claims 68 - 72, 75, 77, 78, 83 - 106, 112, 114, and 124, are also reasonably deemed as readable on elected "species" I.

Traversal of Restriction Requirement

The Restriction Requirement is respectfully traversed.

Firstly, the establishment of "species" I as "A method comprising selecting the varactor of figures 8a, 8b, 8c, 8d, 10a, 10b, 10c, 10d, and 17, wherein the varactor has a an [sic] electrode 116 located opposite to the gate electrode, in those figures" is inappropriate. Based on how Figs. 8 and 10 are illustrated and on how they are described in the specification, none of the limitations of any of the other asserted "species" is excluded in Figs. 8 and 10. Although the claims identified as readable on "species" I do not include claims covering the additional features of Figs. 9a, 9b, 12 - 16, 19, and 21, none of these

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

additional features is excluded in Figs. 8 and 10. For instance, field insulation 134 of Fig. 9b could be used in the varactor of Fig. 8.

In short, Figs. 8 and 10 of "species" I are generic to all the other asserted "species" and, including or separate from Fig. 17, do not form a true "species". By electing "species" I, the claims readable on the elected "species" should consist of all the pending claims. The Restriction Requirement is therefore a nullity.

Secondly, to the extent that all of the pending claims do not read on elected "species" I, certain of the pending claims may not be readable on any of the seven asserted "species". The Restriction Requirement may therefore improperly prevent Applicants from pursuing certain of the pending claims in this application.

More particularly, independent Claim 95 recites that a field insulating region extends "into the semiconductor body along the primary surface to define a semiconductor island laterally surrounded by the field insulating region and substantially fully occupied by material of the plate and body regions". Claim 95 further recites that the gate electrode comprises "multiple gate electrode portions which are of doped semiconductor material and which at least partially overlie the body region" and that each gate electrode portion is "of different conductivity type or/and different average net dopant concentration than each other gate electrode portion". Claim 95 is directed to the varactors such as the implementation of Figs. 37 and 38 in which field insulating region 134 extends along upper semiconductor surface 106 to define semiconductor island 136 substantially fully occupied by material of plate region 102 and body region 100 and in which gate electrode 112 includes n++ portion 112LA and p++ portion 112LB.

"Species" III is, as mentioned above, described as "A method comprising selecting a varactor of figure 9b, wherein a varactor has a two parts [sic] havily [sic] doped semiconductor gate, and also has a semiconductor island which is confined between the two outermost trench insulations shown in the figure". Field insulating region 134 extends along upper semiconductor surface 106 of the varactor shown in Fig. 9b to define semiconductor island 136 substantially fully occupied by material of plate region 102 and body region 100. Gate electrode 112 of the varactor of Fig. 9b includes n++ semiconductor material. However, electrode 112 in Fig. 9b does not have any p-type semiconductor material. Nor

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

does electrode 112 in Fig. 9b include semiconductor portions of different average net dopant concentrations. Consequently, Claim 95 may not read on "species" III.

"Species" V is described as "A method comprising selecting a varactor of figure 14, wherein the gate electrode comprises two heavily doped portions with different conductivity types". Gate electrode 112 in the varactor of Fig. 14 does include n++ portion 112LA and p++ portion 112LB. However, Fig. 14 does not illustrate field insulation 134. As a result, Claim 95 may not read on "species" V.

Aside from "species" I, Claim 95 does not appear to read on any of the other asserted "species". Similar comments apply to independent Claims 83 and 89 dealing with other aspects of varactors having field insulating regions. That is, aside from "species" I, independent Claims 83 and 89 do not appear to read on any of the asserted "species". Unless all of the pending claims are deemed to be readable on elected "species" I, the Restriction Requirement appears to preclude Applicant from pursuing any of independent Claims 83, 89. and 95 and their dependent claims in the present application. This is improper. Hence, either the Restriction Requirement must be withdrawn or all of the pending claims must be deemed readable on elected "species" I.

Thirdly, the Examiner's characterization of certain of the asserted "species" is unduly limiting or/and inaccurate. For example,

a. Fig. 17, which is included in the description of "species" I, presents an implementation of the varactor of Fig. 8 in which portions 126A - 126C of surface depletion region 126 are respectively provided with different progressively increasing values N_{BA}, N_{BB}, and N_{BC} of average net dopant concentration N_B. See paragraph 207 of the specification. Portions 126A - 126C of surface depletion region 126 in the varactor of Fig. 8 may have, but are not required to have, different values of average net dopant concentration N_B. Any inference, based on the inclusion of Fig. 17 in the description of "species" I, that the varactor of Fig. 8 is limited to surface depletion portions 126A - 126C having different average net dopant concentrations is incorrect.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

b. With respect to the recitation in the description of "species" I that " the varactor has a an [sic] electrode 116 located opposite to the gate electrode, in those figures", paragraph 82 of the specification provides that:

> A body electrode 116 electrically contacts body region 100. The contact between body electrode 116 and body region 100 is typically made through one or more heavily doped body contact portions (not separately shown here) of region 100. For simplicity, Fig. 8 illustrates body electrode 116 as contacting region 100 along lower semiconductor surface 108.

The varactor of Fig. 8 thus includes within its ambit the situation of placing body electrode 116 at other suitable locations such as along upper semiconductor surface 106 in the manner depicted in Figs. 9a and 9b. Any inference that the location of body electrode 116 in the varactor of Fig. 8 is limited to the body-electrode location recited in the description of "species" I is inaccurate. The same applies to Fig. 17 and to Fig. 10 with respect to body electrode 166.

c. "Species" II is described as "A method comprising selecting a varactor of figure 9a, wherein the varactor has a two parts [sic], heavily doped semiconductor gate, and has a body electrode 116 located across the gate electrodes in the figure, but not opposite to the gate electrode". As mentioned above, "Species" III is described as "A method comprising selecting a varactor of figure 9b, wherein a varactor has a two parts [sic] havily [sic] doped semiconductor gate, and also has a semiconductor island which is confined between the two outermost trench insulations shown in the figure". Two laterally separated portions of gate electrode 112 are depicted in each of Figs. 9a and 9b. As pointed out in paragraph 139 of the specification, "These two portions can be two laterally separated gate electrodes 112 with gate voltage V_G being applied to each electrode 112". However, as pointed out in the next sentence of paragraph 139, "The two portions can also be connected together outside the plane of Fig. 9a to form a single, normally annular, electrode 112". Any inference that the gate electrode of "species" II or III is limited to multiple laterally separated portions is incorrect.

d. "Species" IV is described as "A method comprising selecting a varactor of figures 12, 13, and 19, wherein the varactor has gate insulators beneath the gate electrode, with two different thicknesses". However, gate dielectric layer 110 is of substantially a constant thickness in the varactor implementation of Fig. 13. The reference to Fig. 13 does not belong in the description of "species" IV.

Fourthly, some of the asserted "species" are unduly narrow and, if the Restriction Requirement is maintained, should be consolidated or examined together regardless of

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

whether they are considered to be patentably distinct inventions. This applies, for example, to "species" IV and VII.

"Species" VII is described as "A method comprising selecting the varactor of figures 16 and 21, wherein the gate insulator has three different thicknesses beneath the gate electrode and the gate electrode is a continuous heavily doped region". By the phrase "the gate electrode is a continuous heavily doped region", the Examiner presumably means that lower gate-electrode layer 112L in Figs. 16 and 21 consists of heavily doped semiconductor material of only one conductivity type.

Lower gate-electrode layer 112L in Figs. 12 and 19 covered in "species" IV consists of heavily doped semiconductor material of only one conductivity type. Consequently, the only material difference between "species" IV and VII is that "species" VII covers one more gate-dielectric thickness than "species" IV. This is a narrow difference. The Examiner's burden in examining "species" IV and VII together should not be much greater that the total burden in examining both of "species" IV and VII separately. If the Restriction Requirement is maintained, "species" IV and VII should be consolidated or examined together. Also, "species" IV and VII should be modified to cover varactor implementations, such as that of Fig. 26, in which there are four or more different gate dielectric thicknesses.

Finally, the Examiner is also the examiner on parent U.S. patent application 10/054,653 in which structure claims corresponding generally to the method claims of the above application are being prosecuted. In particular, structure claims corresponding to all the "species" asserted in the Restriction Requirement are being examined by the present Examiner in the parent application.

The Manual of Patent Examining Procedure states in section 802.01 that "If the search and examination of an entire application can be done without serious burden, the examiner must examine it on the merits, even though it includes claims to independent or distinct inventions". Since structure claims corresponding to all the asserted "species" are being examined by the present Examiner in the parent application, the search and examination of the above application can be done without serious burden to the Examiner. Consequently, the Examiner should examine all the "species" in this application.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

In short, either the Restriction Requirement should be withdrawn or all of the pending claims should be deemed readable on elected "species" I. In either case, all of the asserted "species" should be examined in this application.

Please telephone Applicant's Attorney at 650-964-9767 if there are any questions.

EXPRESS MAIL LABEL NO.:

EV 500 311 222 US

Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicant(s)
Reg. No. 29,089

210 Central Avenue
Mountain View, CA 94043-4869

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779